

MATLAB/simulink modelling and simulation of 9-level cascaded H-bridge multilevel inverter with mismatched DC sources

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ABSTRACT

This paper presents a MATLAB/Simulink model for a 9-level cascaded H-bridge multilevel inverter with mismatched DC voltage sources. The impact of mismatched DC voltage sources on the performance of the 9-level CHBMLI is investigated. Due to the mismatched voltages among DC voltage sources, the output fundamental voltage is different from the input reference voltage. To address this problem, a switching-angle calculation technique that accounts for mismatched as well as varying DC voltage sources is demonstrated. The switching angles obtained using this technique is able to produce the desired output fundamental voltage for a wide range of input reference voltages. Since this switching-angle calculation technique does not require complex iterative computation, it has the potential for real-time implementation.

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1. INTRODUCTION

The power quality of the AC output voltage produced by a 9-level cascaded H-bridge inverter (CHBMLI) shown in Figure 1 is determined by the harmonic contents of the output voltage waveform which can be measured as total harmonic distortion (THD) [1-3]. The presence of harmonics in the output voltage waveform is due to the stepped output voltage levels, given by an example of a staircase waveform in Figure 2. Both the output fundamental voltage and the harmonic contents are related to the switching angles applied to the active power semiconductor switches in the H-bridge (HB) modules. Therefore, it is necessary to calculate the switching angles in order to obtain an output voltage waveform with the desired fundamental voltage and the lowest possible THD [4].

Switching angles are usually calculated off-line and kept in lookup tables for real-time control due to the complex iterative switching-angle calculations involved. The main drawback of this method is that distinct lookup tables are required for each distinct value of output fundamental voltage [5-6]. Also, large sets of lookup tables result in higher cost associated with the hardware required for real-time calculation.

In practice, battery characteristics such as internal resistance and self-discharge rate are different among units [7-10]. Consequently, for battery powered H-bridge cells, the voltages among batteries used as DC voltage sources are mismatched. Several researchers developed various strategies to compensate the mismatch among the batteries. However, the compensation circuits require additional components that increase the circuit complexity.

In this work, a switching-angle calculation technique based on a geometric approach that accounts for mismatched voltages among DC voltage sources for a 9-level CHBML is described in Section 2. The impact of mismatched voltages among DC voltage sources on the performance of the system is highlighted in Section 3. Also, the effectiveness of the presented switching-angle calculation technique validated via a 9-level CHBML MATLAB/Simulink model is demonstrated in Section 3.

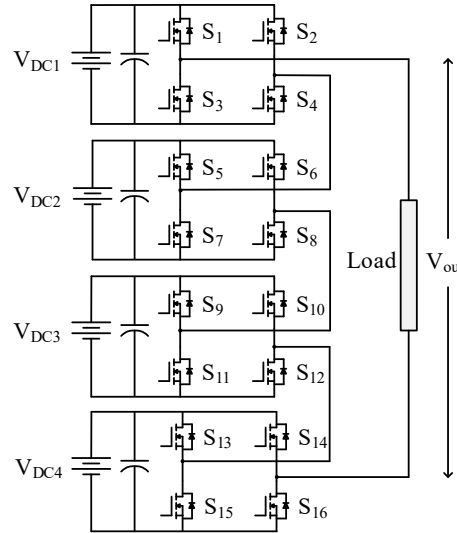


Figure 1. A typical 9-level CHBML

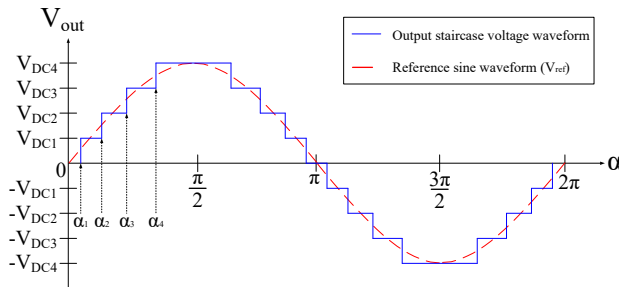


Figure 2. Staircase voltage waveform produced by 9-level CHBML

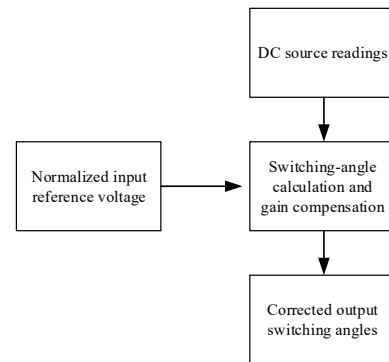


Figure 3. Switching-angle calculation algorithm for 9-level CHBML with mismatched DC voltage sources

2. SWITCHING-ANGLE CALCULATION TECHNIQUE

Figure 3 shows the block diagram of the control algorithm, which includes a gain compensation for a 9-level CHBML. The switching angles are determined from the reference voltage, V_{ref_pk} , as follows:

$$\sin(\alpha_n) = \frac{\pi[(V_{DC} + \Delta V_{DCn}) + 2\{(V_{DC} + \Delta V_{DC1}) + \dots + (V_{DC} + \Delta V_{DC(n-1)})\}]}{2V_{ref_pk}} \quad (1)$$

where V_{DC} is the nominal voltage of the individual DC voltage sources, ΔV_{DC} is the variation of the individual DC voltage sources, and α_n is the n -th switching angle. The relation between the output

fundamental voltage, V_1 , and the switching angles can be obtained by analysing the output voltage using Fourier series. The expression of the fundamental voltage can be written as:

$$V_1 = \frac{4}{\pi} [V_{DC1} \cos \alpha_1 + V_{DC2} \cos \alpha_2 + V_{DC3} \cos \alpha_3 + V_{DC4} \cos \alpha_4] \quad (2)$$

$$\begin{aligned} V_{DC1} &= V_{DC} \pm \Delta V_{DC1} \\ V_{DC2} &= V_{DC} \pm \Delta V_{DC2} \\ V_{DC3} &= V_{DC} \pm \Delta V_{DC3} \\ V_{DC4} &= V_{DC} \pm \Delta V_{DC4} \end{aligned}$$

where

The limitation of (1) to produce the switching angles needed to produce the desired output fundamental voltage can be proofed by using (2). The conditions are set as follows: All the DC voltage sources are set to 10 V and the input reference voltage is set to 37.2 V. By using (1), the switching angles obtained for a 9-level CHBML shown in Figure 1 are: $\alpha_1=7.73^\circ$, $\alpha_2=23.79^\circ$, $\alpha_3=42.26^\circ$ and $\alpha_4=70.30^\circ$. Using (2), the output fundamental voltage, V_1 , obtained from these switching angles is 38.0 V, which is different from the input reference voltage. To obtain the desired output fundamental voltage with minimal error, it is necessary to perform a gain compensation, as shown by the control algorithm given in Figure 3. The expression of the output fundamental voltage with compensation can be obtained by rewriting (2):

$$V_{1_out} = \frac{4}{\pi} [V_{DC1} \cos(\alpha_1 \pm \Delta \alpha_1) + V_{DC2} \cos(\alpha_2 \pm \Delta \alpha_2) + V_{DC3} \cos(\alpha_3 \pm \Delta \alpha_3) + V_{DC4} \cos(\alpha_4 \pm \Delta \alpha_4)] \quad (3)$$

where V_{1_out} is the corrected output fundamental voltage after gain compensation and $\Delta \alpha$ is compensation of switching angles to produce the desired output fundamental voltage. From the equations above, the corrected output fundamental voltage can be rewritten in terms of input reference voltage and the switching angles as follows:

$$V_{1_out} = \frac{4}{\pi} [\beta_1 V_{DC1} + \beta_2 V_{DC2} + \beta_3 V_{DC3} + \beta_4 V_{DC4}] + V_{ref_pk} \quad (4)$$

$$\begin{aligned} \beta_1 &= \cos(\alpha_1 + \Delta \alpha_1) - \cos(\alpha_1) \\ \beta_2 &= \cos(\alpha_2 + \Delta \alpha_2) - \cos(\alpha_2) \\ \beta_3 &= \cos(\alpha_3 + \Delta \alpha_3) - \cos(\alpha_3) \\ \beta_4 &= \cos(\alpha_4 + \Delta \alpha_4) - \cos(\alpha_4) \end{aligned}$$

where

To produce the desired output fundamental voltage while considering the mismatched voltages among the DC voltage sources, the switching angles are first obtained by using (1) and then, compensation is performed by using (4).

3. SIMULATION RESULTS

The system has been verified using MATLAB for normalized output fundamental voltage range from 0.00 to 1.00. To verify the impact of mismatched voltages among the DC sources on the performance of the system and the effectiveness of the algorithm to account for mismatched voltages among DC voltage sources, the algorithm is tested for a 9-level CHBML with mismatched DC voltage sources. The switching angles are first calculated using Equation (1) and (4), assuming that all DC voltage sources are equal and perfectly matched to a 10 V nominal voltage. The switching angles are then used to calculate the output fundamental voltage of 9-level CHBML with DC voltage sources mismatched to $\pm 20\%$ of the nominal voltage to investigate the impact of the mismatched DC voltage sources onto the performance of the system.

Figure 4 shows the normalized output fundamental voltage versus the normalized input reference voltage for 9-level CHBML. From the results obtained, without taking into consideration the mismatched DC voltage sources, the output fundamental voltage differs from the desired output fundamental voltage defined by the input reference voltage. After considering the mismatched voltages among the DC voltage sources, the

output fundamental voltage is very close to the desired output fundamental voltage given by the input reference voltage.

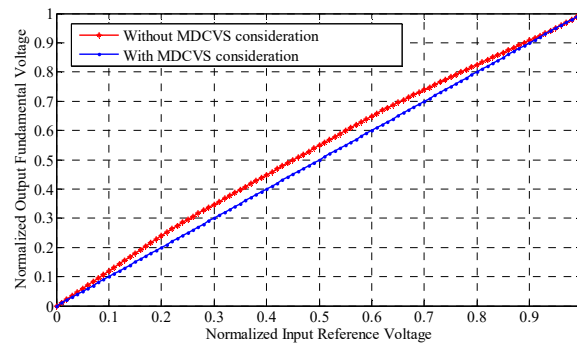


Figure 4. Comparison between normalized output fundamental voltage without and with mismatched DC voltage sources (MDCVS) consideration for 9-level CHBMI

Figure 5 shows the switching angles versus normalized output fundamental voltage for a 9-level CHBMI, whilst Figure 6 shows the THD versus normalized output fundamental voltage for a 9-level CHBMI. At the lowest range of output fundamental voltage, the THD increases due to reduced available output voltage levels. Whilst at the highest range of the output fundamental voltage, the THD increases due to the output voltage waveform approaches a square wave.

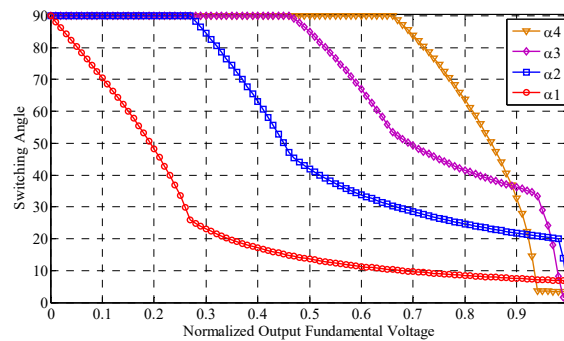


Figure 5. Switching angle trajectories after gain compensation for 9-level CHBMI with $\pm 20\%$ voltage mismatch from the nominal voltage of the DC voltage sources

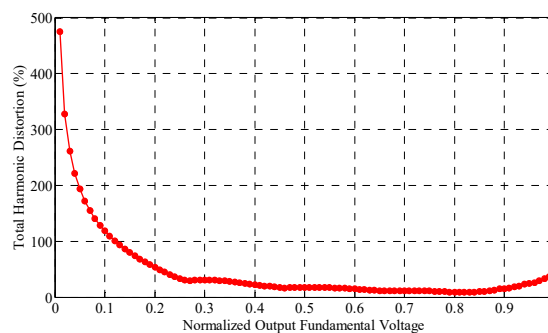


Figure 6. THD of output voltage waveform for 9-level CHBMI with $\pm 20\%$ voltage mismatch from the nominal voltage of the DC voltage sources

To verify the effectiveness of the presented switching-angle calculation technique to account for the mismatched voltages among DC voltage sources, a MATLAB/Simulink model of 9-level CHBML with mismatched DC voltage sources has been built and tested. The model is shown in Figure 7. In the model, all DC voltage sources are assumed to have a 10 V nominal voltage and $\pm 20\%$ voltage mismatch from its nominal voltage. The resistance and inductance of the inductive load used in the MATLAB/Simulink model are $10\ \Omega$ and $28\ \text{mH}$, respectively. To test the model, a normalized input reference voltage initially set to 0.80 is stepped down to 0.60 after 0.2 s, as given by an example in Figure 8(a). The resultant output voltage and output current waveforms associated with the normalized input reference voltages of 0.80 and 0.60 are shown in Figure 8(b) and Figure 8(c), respectively. From Figure 8(a), 8(b), and 8(c), it is clearly shown that the amplitudes of the output voltage and the output current waveforms are reduced after the normalized input voltage reference is stepped down from 0.80 to 0.60, suggesting that the model is able to correctly respond and track the time-varying voltage demand.

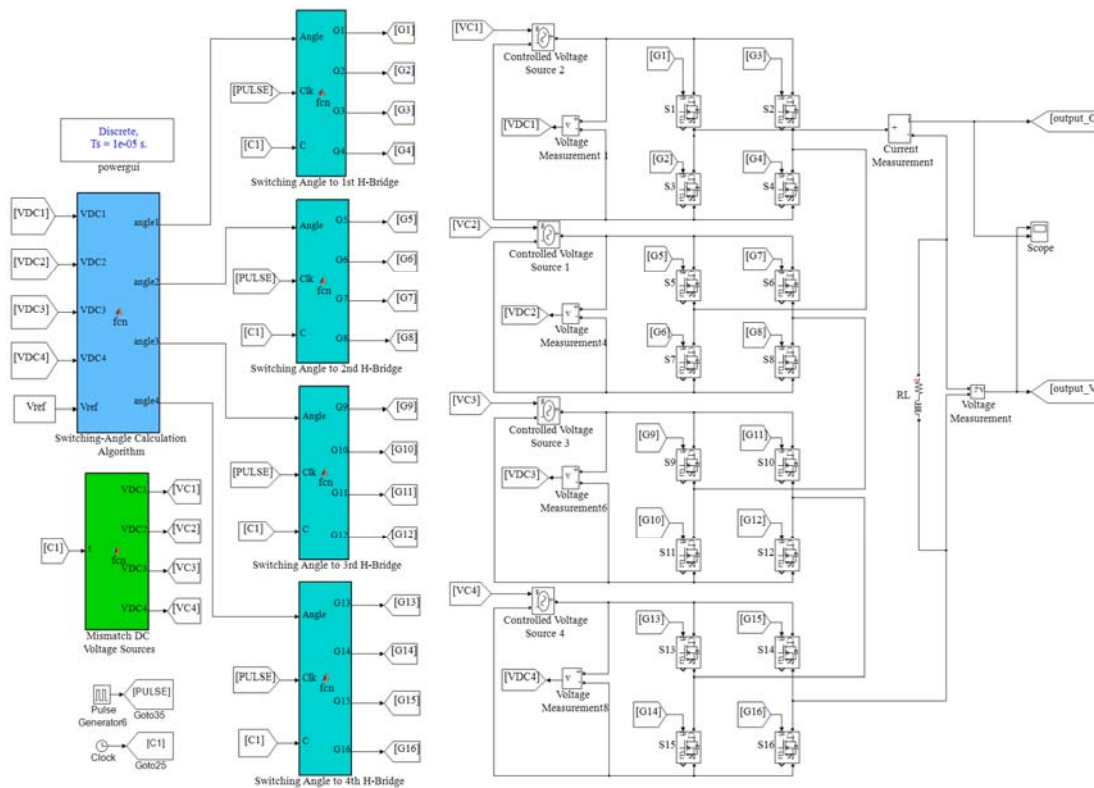
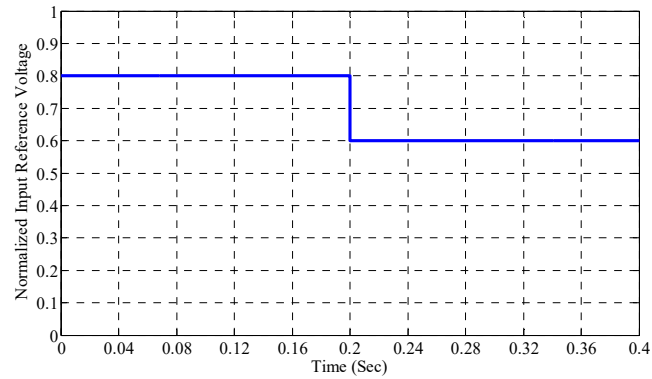
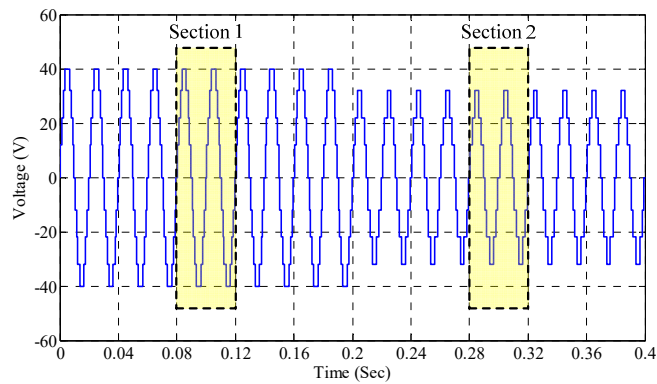


Figure 7: MATLAB/Simulink model of 9-level CHBML with mismatched DC voltage sources

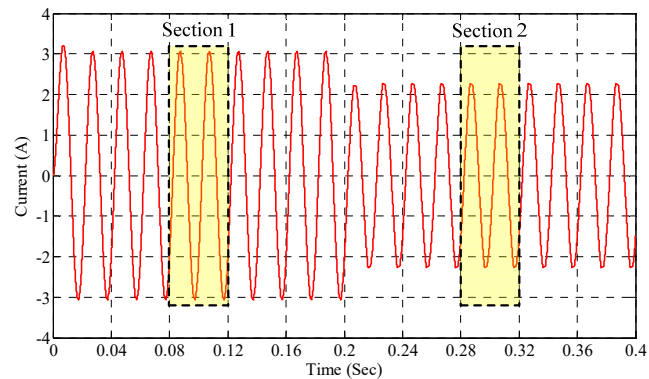
For clarity, a close-up view of the output voltage and the output current waveforms shown in Section 1 in Figure 8(b) and 8(c), respectively, for the normalized input reference voltage of 0.80 is given in Figure 9. The harmonic contents of the output voltage and output current waveforms in Figure 9 that are obtained through Fast Fourier Transform (FFT) analysis are shown in Figure 10(a) and 10(b), respectively.



(a)



(b)



(c)

Figure 8. (a) Normalized input reference voltages of 0.80 and 0.60 against time, (b) the associated output voltage waveform produced by 9-level CHBMI with $\pm 20\%$ voltage mismatch from the nominal voltage of the DC voltage sources and (c) the associated output current waveform produced by 9-level CHBMI with $\pm 20\%$ voltage mismatch from the nominal voltage of the DC voltage sources

Figure 10(a), the output fundamental voltage is 40.74 V. This value is identical to the actual input reference voltage of 40.74 V for the normalized input reference voltage of 0.80. Comparing Figure 10(b) with Figure 10(a), the harmonic contents of the output current waveform are found to be lower than those of the output voltage waveform. The reason is that the inductive characteristic of the load filters part of the

harmonics, and therefore, the output current has lower harmonic contents. Similarly, for normalized input reference voltage of 0.60, a close-up view of the output voltage and output current waveforms shown in Section 2 in Figure 8(b) and 8(c) is given in Figure 11. The harmonic contents of the output voltage and output current waveforms obtained via FFT analysis are shown in Figure 12 (a) and 12(b), respectively. The output fundamental voltage obtained from the FFT analysis is 30.56 V, and this value, again, is identical to the actual input reference voltage, i.e. 30.56 V for the normalized input reference voltage of 0.60. Note that, in both cases, the output fundamental voltages obtained under time varying voltage demand are identical to the respective input reference voltages. These results therefore clearly demonstrate the effectiveness of the presented switching-angle calculation technique to account for the mismatched voltages among DC voltage sources. Being able to respond to time-varying voltage demand and produce the desired output fundamental voltage, this technique has the potential for real-time implementation.

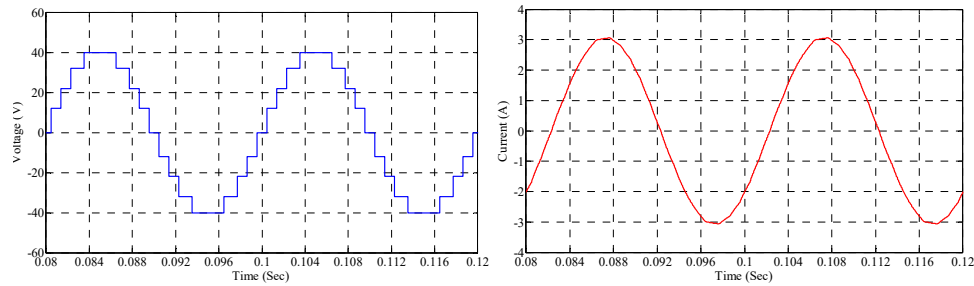


Figure 9. Close-up view of the output voltage and output current waveforms at Section 1 for normalized input reference voltage of 0.80

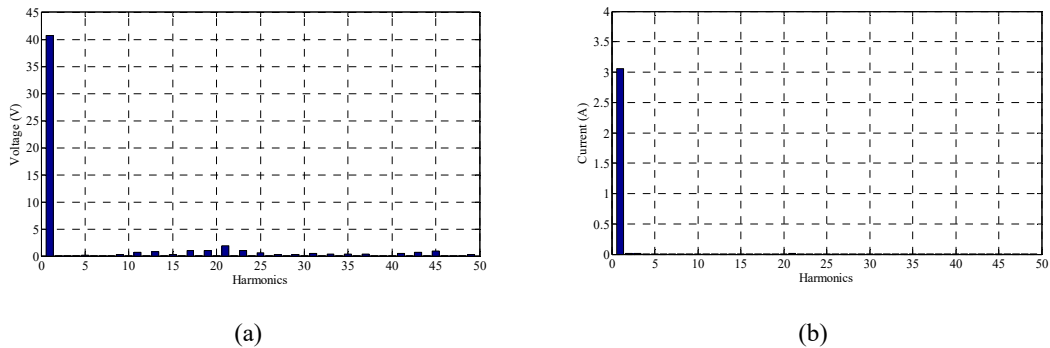


Figure 10. (a): FFT analysis of output voltage waveform for normalized input reference voltage of 0.80 and (b) FFT analysis of output current waveform for normalized input reference voltage of 0.80

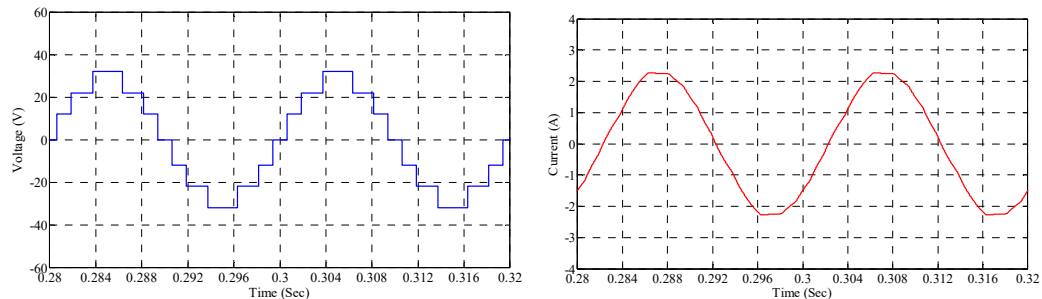


Figure 11. Close-up view of output voltage and output current waveforms at Section 2 for normalized input reference voltage of 0.60

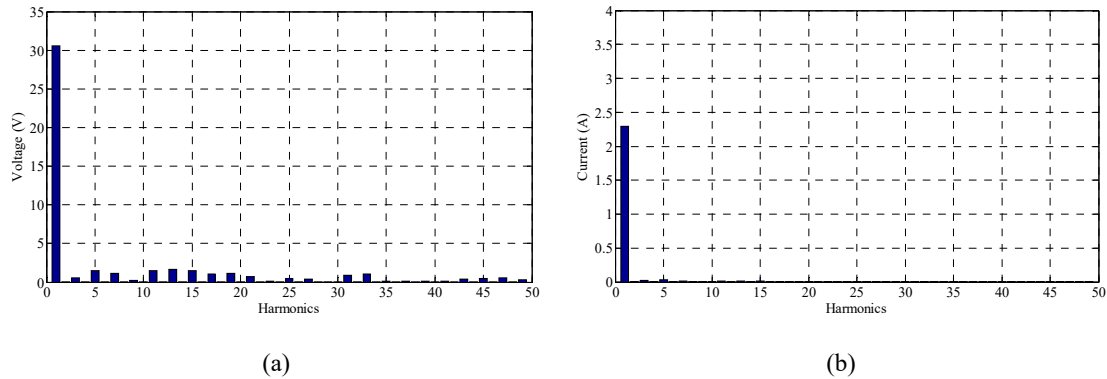


Figure 12. (a) FFT analysis of output voltage waveform for normalized input reference voltage of 0.60 and (b) FFT analysis of output current waveform for normalized input reference voltage of 0.6

4. CONCLUSION

The impact of mismatched voltages among DC voltage sources on the performance of 9-level CHBMI is presented. Due to the mismatched voltages, the output fundamental voltage is different from the input reference voltage. To overcome this problem, a switching-angle calculation technique based on a geometric approach is demonstrated. By taking into account the mismatched voltages among DC voltage sources, this technique is able to produce a set of switching angles needed to produce the desired output fundamental voltage. This technique can be employed for a wide range of input reference voltages. The ability of the MATLAB/Simulink model of 9 level CHBMI to produce the desired output fundamental voltage under time-varying voltage demand clearly demonstrates the effectiveness of the switching-angle calculation technique to account for mismatched voltages among DC voltage sources. Since this technique does not require complex iterative computation, it is expected that the technique can be implemented in real-time. The hardware prototype will be developed to validate the simulation results and the results will be published elsewhere.

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